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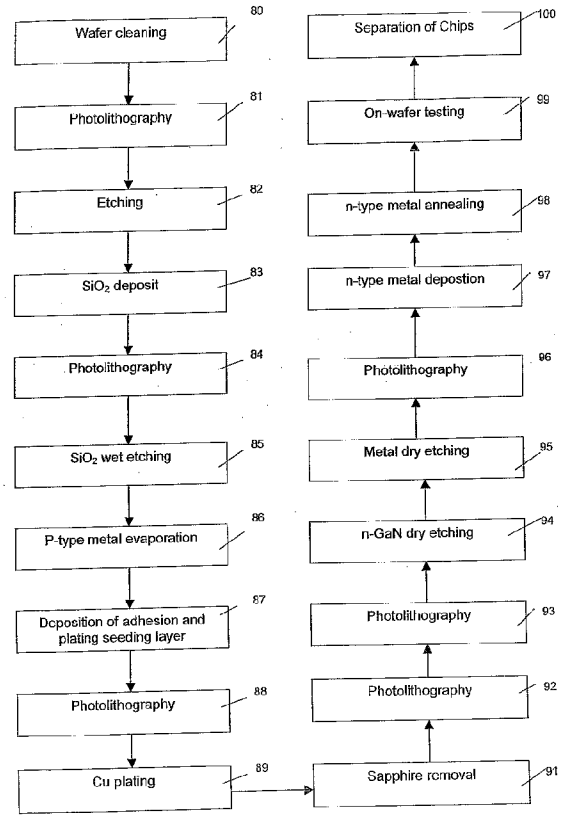
(54) Title: FABRICATION OF SEMICONDUCTOR DEVICES



(57) Abstract: A method for fabrication of a semiconductor device on a substrate, the semiconductor having a wafer. The methodincludes the steps:(a) applying a seed layer of a thermally conductive metal to the wafer;(b) electroplating a relatively thick layer of the conductive metal on the seed layer; and(c) removing the substrate.A corresponding semiconductor device is also disclosed.

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Fabrication of Semiconductor Devices

Field of the Invention

The present invention relates to the fabrication of semiconductor devices and refers particularly, though not exclusively, to the plating of a heat sink on the semiconductor device.

Background to the Invention

As semiconductor devices have developed there has been a considerable increase in their operational speed, and a reduction in overall size. This is causing a major problem of heat build-up in the semiconductor devices. Therefore, heat sinks are being used to help dissipate the heat from the semiconductor device. Such heat sinks are normally fabricated separately from the semiconductor device and are normally adhered to the semiconductor device just prior to encapsulation.

There have been many proposals for the electroplating of copper onto surfaces of semiconductor devices during their fabrication, particularly for use as interconnects.

The majority of current semiconductor devices are made from semiconductor materials based on silicon (Si), gallium arsenide (GaAs), and indium phosphide (InP). Compared to such electronic and optoelectronic devices, GaN devices have many advantages. The major intrinsic advantages that GaN have are summarised in Table 1:

Semi-conductor	Mobility μ (cm^2/Vs)	Band Gap (eV)/ wavelength (nm)	BFOM (power transistor merit)	Maximum Temperature (C)
Si	1300	1.1/1127	1.0	300
GaAs	5000	1.4/886	9.6	300
GaN	1500	3.4/360	24.6	700

Table 1

From Table 1, it can be seen that GaN has the highest band gap (3.4 eV) among the given semiconductors. Thus, it is called a wide band gap semiconductor. Consequently, electronic devices made of GaN operate at much higher power than Si and GaAs and InP devices.

For semiconductor lasers, GaN lasers have a relatively short wavelength. If such lasers are used for optical data storage, the shorter wavelength may lead to a higher capacity. GaAs lasers are used for the manufacture of CD-ROMs with a capacity of about 670 MB/disk. AlGaInP lasers (also based on GaAs) are used for the latest DVD players with a capacity of about 4.7 GB/disk. GaN lasers in the next-generation DVD players may have a capacity of 26 GB/disk.

GaN devices are made from GaN wafers that are typically multiple GaN-related epitaxial layers deposited on a sapphire substrate. The sapphire substrate is usually two inches in diameter and acts as the growth template for the epitaxial layers. Due to lattice mismatch between GaN-related materials (epitaxial films) and sapphire, defects are generated in the epitaxial layers. Such defects cause serious problems for GaN lasers and transistors and, to a lesser extent, for GaN LEDs.

There are two major methods of growing epitaxial wafers: molecular beam epitaxy (MBE), and metal organic chemical vapour deposition (MOCVD). Both are widely used.

Conventional fabrication processes usually include these major steps: photolithography, etching, dielectric film deposition, metallization, bond pad formation, wafer inspection/testing, wafer thinning, wafer dicing, chip bonding to packages, wire bonding and reliability testing.

Once the processes for making LEDs are completed at the full wafer scale, it is then necessary to break the wafer into individual LED chips or dice. For GaN wafers grown on sapphire substrates, this "dicing" operation is a major problem as sapphire is very hard. The sapphire first has to be thinned uniformly from about 400 microns to about 100 microns. The thinned wafer is then diced by diamond scriber, sawed by a diamond saw or by laser grooving, followed by scribing with diamond scribers. Such processes limit throughput, cause yield problems and consume expensive diamond scribers/saws.

Known LED chips grown on sapphire substrates require two wire bonds on top of the chip. This is necessary because sapphire is an electrical insulator and current conduction through the 100-micron thickness is not possible. Since each wire bond pad takes about 10-15% of the wafer area, the second wire bond reduces the number of chips per wafer by about 10-15% as compared to single-wire bond LEDs grown on conducting substrates. Almost all non-GaN LEDs are grown on conducting substrates and use one wire bond. For packaging companies, two wire bonding reduces packaging yield, requires modification of one-wire bonding processes, reduces the useful area of the chip, and complicates the wire bonding process and thus lowers packaging yield.

Sapphire is not a good thermal conductor. For example, its thermal conductivity at 300K (room temperature) is 40W/Km. This is much smaller than copper's thermal conductivity of 380 W/Km. If the LED chip is bonded to its package at the sapphire interface, the heat generated in the active region of the device must flow through 3 to 4 microns of GaN and 100 microns of sapphire to reach the package/heat sink. As a consequence, the chip will run hot affecting both performance and reliability.

For GaN LEDs on sapphire, the active region where light is generated is about 3-4 micron from the sapphire substrate.

Summary of the Invention

In accordance with a preferred form of the present invention, there is provided a method for fabrication of a semiconductor device on a substrate, the semiconductor device having wafer with a device layer; the method including the steps:

(a) electroplating a layer of a thermally conductive material onto a surface of the wafer remote from the substrate and close to the device layer; and

(b) removing the substrate.

The semiconductor device may be a silicon-based device.

In accordance with another form, there is provided a method for fabrication of a light emitting device on a substrate, the light emitting device having wafer with an active layer; the method including the steps:

(a) electroplating a layer of a thermally conductive material onto a surface of the wafer remote from the substrate and close to the active layer; and

(b) removing the substrate.

For both forms, the thermally conductive layer may be as a heat sink, and may be of a thickness in the range of from 3 microns to 300 microns, preferably 50 to 200 microns.

In a further form, the present invention provides a method for fabrication of a semiconductor device on substrate, the semiconductor device having a wafer; the method including the steps:

(a) applying a seed layer of a thermally conductive metal to a first surface of the wafer remote from the substrate;

(b) electroplating a relatively thick layer of the thermally conductive metal on the seed layer; and

(c) removing the substrate.

Prior to the seed layer being applied, the wafer may be coated with an adhesion layer. Before the electroplating of the relatively thick layer the seed layer may be patterned with photoresist patterns; the relatively thick layer being electroplated between the photoresists.

The seed layer may be electroplated without patterning and with patterning being performed subsequently. Patterning may be by photoresist patterning and then wet etching. Alternatively, it may be by laser beam micro-machining of the relatively thick layer.

Between steps (b) and (c) there may be performed the additional step of annealing the wafer to improve adhesion.

Preferably, the photoresists are of a height of at least 15 to 500 microns, more preferably 50 to 200 microns, and have a thickness in the range 3 to 500 microns. More preferably, the photoresists have a spacing in the range of 200 to 2,000 microns, preferably 300 microns.

The relatively thick layer may be of a height no greater that the photoresist height. Alternatively, the conductive metal layer may be electroplated to a height greater than the photoresist and be subsequently thinned. Thinning may be by polishing or wet etching.

After step (c) there may be included an extra step of forming on a second surface of the wafer remote from the relatively thick layer, a second ohmic contact layer. The contact layer may be a second ohmic contact layer. The second ohmic contact layer may be one of opaque, transparent, and semi-transparent, and may be either blank or patterned. Ohmic contact formation and subsequent process steps may be carried out. The subsequent process steps may include deposition of wire bond pads. The exposed second surface of the wafer layer may be cleaned and etched before the second ohmic contact layer is deposited onto it. The second ohmic contact layer may not cover the whole area of the second surface of the wafer.

The semiconductor devices may be tested on the wafer, and the wafer may be subsequently separated into individual devices.

The semiconductor devices may be fabricated without one or more of: lapping, polishing and dicing.

The wafer may include epitaxial layers and, on the epitaxial layers remote from the substrate, first ohmic contact layers. The first ohmic contact layers may be on p-type layers of the epitaxial layers; and the second ohmic contact layer may be formed on n-type layers of the expitaxial layers.

After step (c), dielectric films may be deposited on the epitaxial layers. Openings may then be cut in the dielectric and second ohmic contact layer and bond pads deposited on the epitaxial layers. Alternatively, after step (c), electroplating of a thermally conductive metal (or other material) on the epitaxial layers may be performed.

The invention is also directed to a semiconductor device fabricated by the above method. The invention, in a preferred aspect, also provides a light emitting diode or a laser diode fabricated by the above method.

In a further aspect, the present invention provides a semiconductor device comprising epitaxial layers, a first ohmic contact layer on a first surface of the epitaxial layers, a relatively thick layer of a thermally conductive metal on the first ohmic contact layer, and a second ohmic contact layer on a second surface of the epitaxial layers; the relatively thick layer being applied by electroplating.

There may be an adhesive layer on the first ohmic contact layer between the first ohmic contact layer and the relatively thick layer.

The relatively thick layer may be at least 50 micrometers thick; and the second ohmic contact layer may be a thin layer in the range of from 3 to 500 nanometers. The second ohmic contact layer may be transparent, semi-transparent or opaque; and may include bonding pads.

For all forms of the invention, the thermally conductive metal may be copper.

There may be a seed layer of the thermally conductive metal applied to the adhesive layer.

The semiconductor device may be one of: a light emitting diode, a laser diode, and a transistor device.

In yet another form, there is provided a semiconductor device comprising epitaxial layers, a first ohmic contact layer on a first surface of the epitaxial layers, an adhesive layer on the first ohmic contact layer, and a seed layer of a thermally conductive metal on the adhesive layer.

There may be further included a relatively thick layer of the thermally conductive metal on the seed layer.

A second ohmic contact layer may be provided on a second surface of the epitaxial layers; the second ohmic contact layer being a thin layer in the range of from 3 to 500 nanometers. The second ohmic contact layer may comprise bonding pads; and may be one of: opaque, transparent, and semi-transparent.

The thermally conductive metal may comprise copper; and the epitaxial layers may comprise GaN-related layers.

The semiconductor device may be a light emitting device.

In a penultimate form, the present invention provides a method of fabrication of a semiconductor device, the method including the steps:

(a) on a substrate with a wafer comprising multiple GaN-related epitaxial layers, forming a first ohmic contact layer on a first surface of the wafer;

(b) removing the substrate from the wafer; and

(c) forming a second ohmic contact layer on a second surface of the wafer, the second ohmic contact layer having bonding pads formed thereon.

The second ohmic contact layer may be for light emission; and may be opaque, transparent, or semi-transparent. The second ohmic contact layer may be blank or patterned.

In a final form, there is provided a semiconductor device fabricated by the above method.

The semiconductor device may be a light emitting diode or a laser diode.

Brief Description of the Drawings

In order that the invention may be better understood and readily put into practical effect there shall now be described by way of non-limitative example only a preferred embodiment of the present invention, the description being with reference to the accompanying illustrative (and not to scale) drawings in which:

Figure 1 is a schematic representation of a semiconductor device at a first stage in the fabrication process;

Figure 2 is a schematic representation of the semiconductor device of Figure 1 at a second stage in the fabrication process;

Figure 3 is a schematic representation of the semiconductor device of Figure 1 at a third stage in the fabrication process;

Figure 4 is a schematic representation of the semiconductor device of Figure 1 at a fourth stage in the fabrication process;

Figure 5 is a schematic representation of the semiconductor device of Figure 1 at a fifth stage in the fabrication process;

Figure 6 is a schematic representation of the semiconductor device of Figure 1 at a sixth stage in the fabrication process;

Figure 7 is a schematic representation of the semiconductor device of Figure 1 at the seventh stage in the fabrication process; and
Figure 8 is a flow chart of the process.

Detailed Description of the Preferred Embodiment

For the following description, the reference numbers in brackets refer to the process steps in Figure 8.

To refer to Figure 1, there is shown the first step in the process – the metallization on the p-type surface of the wafer 10.

The wafer 10 is an epitaxial wafer with a substrate and a stack of multiple epitaxial layers 14 on it. The substrate 12 can be, for example, sapphire, GaAs, InP, Si, and so forth. Henceforth a GaN sample having GaN layer(s) 14 on sapphire substrate 12 will be used as an example. The epitaxial layers 14 (often called epilayers) are a stack of multiple layers, and the lower part 16 (which is grown first on the substrate) is usually n-type layers and the upper part 18 is often p-type layers.

On GaN layers 14 is an ohmic contact layer 20 having multiple metal layers. To ohmic contact layer 20 is added an adhesion layer 22, and a thin copper seed layer 24 (Figure 2) (step 88) of a thermally conductive metal such as, for example, copper. The thermally conductive metal is preferably also electrically conductive. The stack of adhesion layers may be annealed after formation.

The ohmic layer 20 may be a stack of multiple layers deposited and annealed on the semiconductor surface. It may not be part of the original wafer. For GaN, GaA, and InP devices, the epitaxial wafer often contains an active region that is sandwiched between n-type and p-type semiconductors. In most cases the top layer is p-type. For silicon devices, epitaxial layers may not be used, but just the wafer.

As shown in Figure 3, using standard photolithography (89), the thin copper seed layer 24 is patterned with relatively thick photoresists 26. The photoresist patterns 26 are preferably of a height in the range of 3 to 500 micrometers, preferably 15 to 500 micrometers; and with a thickness of about 3 to 500 micrometers. They are preferably separated from each other by a spacing in the range of 200 to 2,000

microns, preferably 300 microns, depending on the design of the final chips. The actually pattern depends on device design.

A patterned layer 28 of copper is then electroplated onto layer 24 (90) between photoresists 26 to form a heat sink that forms a part of the substrate. The copper layer 28 is preferably of a height no greater than that of the photoresists 26 and is therefore of the same or lesser height than the photoresists 26. However, the copper layer 28 may be of a height greater than that of the photoresists 26. In such a case, the copper layer 28 may be subsequently thinned to be of a height no greater than that of the photoresists 26. Thinning may be by polishing or wet etching. The photoresists 26 may or may not be removed after the copper plating. Removal may be by a standard and known method such as, for example, resin in the resist stripper solution, or by plasma aching.

Depending on the device design, processing of the epitaxial layers 14 follows using standard processing techniques such as, for example, cleaning (80), lithography (81), etching (82), device isolation (83), passivation (84), metallization (85), thermal processing (86), and so forth. (Figure 4). The wafer 10 is then annealed (87) to improve adhesion.

The epitaxial layer 14 is usually made of n-type layers 16 on the original substrate 12; and p-type layers on the original top surface 18 which is now covered with the ohmic 20, adhesion 22 and copper seed layers 24 and the electroplated thick copper layer 28.

In Figure 5, the original substrate layer 12 is then removed (91) using, for example, the method of Kelly [M.K. Kelly, O. Ambacher, R. Dimitrov, R. Handschuh, and M. Stutzmann, phys. stat. sol. (a) 159, R3 (1997)]. The substrate may also be removed by polishing or wet etching.

Figure 6 is the penultimate step and is particularly relevant for light emitting diodes where a transparent ohmic contact layer 30 is added beneath epitaxial layers 14 for light emission. Bonding pads 32 are also added. The Ohmic contact layer 30 is preferably transparent or semi-transparent. It is more preferably a thin layer and may be in the range of 3 to 50 nm thick.

Prior to adding ohmic contact layer 30, known preliminary processes may be performed. These may be , for example, photolithography (92, 93), dry etching (94, 95), and photolithography (96).

Annealing (98) may follow the deposition of ohmic contact layer 30.

The chips/dies are then tested (99) by known and standard methods. The chips/dies can then be separated (100) (Figure 7) into individual devices/chips 1 and 2 without lapping/polishing the substrate, and without dicing. Packaging follows by standard and known methods.

The top surface of the epitaxial layer 14 is preferably in the range of about 0.1 to 2.0 microns, preferably about 0.3 microns, from the active region. For silicon-based semiconductors, the top surface of the semiconductor is preferably in the range 0.1 to 2.0 microns, preferably about 0.3 microns, from the device layer. As the active layer/device layer in this configuration is close to a relatively thick copper pad 28, the rate of heat removal is improved.

Additionally or alternatively, the relatively thick layer 28 may be used to provide mechanical support for the chip. It may also be used to provide a path for heat removal from the active region/device layer, and may also be used for electrical connection.

The plating step is performed at the wafer level (i.e., before the dicing operation) and may be for several wafers at the one time.

The fabrication of GaN laser diodes is similar to the fabrication of GaN LEDs, but more steps may be involved. One difference is that GaN laser diodes require mirror formation during the fabrication. Using sapphire as the substrate compared to the method without sapphire as the substrate, the mirror formation is much more difficult and the quality of the mirror is generally worse.

After sapphire is removed, the laser will have better performance. An example of a typical GaN laser epitaxial wafer structure is shown in Table 2.

Mg doped p-type GaN contact layer	0.15μm
Mg doped p-type $Al_{c.1b}Ga_{0.85}N$ cladding layer	0.45μm
Mg doped p-type GaN wave guiding layer	0.12μm
Mg doped p-type $Al_{0.2}Ga_{0.8}N$ electron blocking layer	200
$In_{0.03}Ga_{0.97}N/In_{0.15}Ga_{0.85}N$ 3-period MQWs active layer	
$In_{0.15}GaN_{0.85}N$ well layer	35□
$In_{0.03}Ga_{0.97}N$ barrier layer	50□
Si doped n-type GaN wave guiding layer	0.12μm
Si doped n-type $Al_{0.15}Ga_{0.85}N$ cladding layer	0.45μm
Si doped n-type $In_{0.1}Ga_{0.9}N$	500 □
Si doped n-type GaN contact layer	3μm
Un-doped n-type GaN	1μm
Un-doped n-type ELO GaN layer	6μm
Un-doped GaN template layer / Si_3N_4 mask	2μm
GaN buffer	300
Sapphire substrate	450μm

Table 2

For standard commercial GaN LEDs, about 5% light generated in the semiconductor is emitted. Various ways have been developed to extract more light out from the chip in non-GaN LEDs (especially red LEDs based on AlGaInP, not GaN).

The first ohmic contact layer 20, being metal and relatively smooth, is quite shinny and therefore highly reflective of light. As such the first ohmic contact layer 20, at its junction with the epitaxial layers 14, also is a reflective surface, or mirror, to improve light output.

Although reference is made to copper, any other platable material may be used provided it is electrically and/or heat conductive, or provides the mechanical support for the semiconductor device.

Whilst there has been described in the foregoing description a preferred form of the present invention, it will be understood by those skilled in the technology that many variations or modifications in design, construction or operation may be made without departing from the present invention.

The claims:

1. A method for fabrication of a semiconductor device on substrate, the semiconductor device having a wafer; the method including the steps:
   (a) applying a seed layer of a thermally conductive metal to a first surface of the wafer;
   (b) electroplating a relatively thick layer of the thermally conductive metal on the seed layer; and
   (c) removing the substrate.

2. A method as claimed in claim 1, wherein the first surface is coated with an adhesion layer prior to application of the seed layer.

3. A method as claimed in claim 1 or claim 2, wherein the seed layer is patterned with photoresist patterns before the electroplating step (b).

4. A method as claimed in claim 3, wherein the electroplating of the relatively thick layer is between the photoresist patterns.

5. A method as claimed in any one of claims 1 to 4, wherein between steps (b) and (c) there is performed the additional step of annealing the wafer to improve adhesion

6. A method as claimed in claim 3 or claim 4, wherein the photoresist patterns are of a height in the range 15 to 500 micrometers.

7. A method as claimed in claim 3 wherein the photoresist patterns have a thickness in the range 3 to 500 micrometers.

8. A method as claimed in any one of claims 3, 4, 6 and 7, wherein the photoresist patterns have a spacing in the range of 200 to 2,000 microns.

9. A method as claimed in any one of claims 1 to 8, wherein the seed layer is electroplated in step (b) without patterning, patterning being performed subsequently.

10. A method as claimed in claim 9, wherein patterning is by photoresist patterning and then wet etching.

11. A method as claimed in claim 9, wherein patterning is by laser beam micro-machining of the relatively thick layer.

12. A method as claimed in any one of claims 3 to 11, wherein the relatively thick layer is of a height no greater that the photoresist height.

13. A method as claimed in any one of claims 3 to 11, wherein the relatively thick layer of thermally conductive metal is electroplated to a height greater than the photoresist and is subsequently thinned.

14. A method as claimed in claim 13, wherein thinning is by polishing or wet etching.

15. A method as claimed in any one of claims 1 to 14, wherein after step (c) there is included an extra step of forming on a second surface of the wafer a second ohmic contact layer, the second ohmic contact layer being selected from the group consisting of: opaque, transparent, and semi-transparent.

16. A method as claimed in claim 15, wherein the second ohmic contact layer is one of blank and patterned.

17. A method as claimed in claim 15 or claim 16, wherein bonding pads are formed on the second ohmic contact layer.

18. A method as claimed in any one of claims 1 to 14, wherein after step (c) ohmic contact formation and subsequent process steps are carried out, the subsequent process steps including deposition of wire bond pads.

19. A method as claimed in claim 18, wherein the exposed second surface is cleaned and etched before the ohmic contact layer is deposited.

20. A method as claimed in any one of claims 15 to 19, wherein the second ohmic contact layer does not cover the whole area of the second surface.

21. A method as claimed in any one of claims 15 to 20, wherein after forming the second ohmic contact layer there is included testing of the semiconductor devices on the wafer.

22. A method as claimed in any one of claims 15 to 21, wherein there is included the step of separating the wafer into individual devices.

23. A method as claimed in any one of claims 1 to 22, wherein the semiconductor devices are fabricated without one or more selected from the group consisting of: lapping, polishing and dicing.

24. A method as claimed in any one of claims 1 to 23, wherein the wafer includes epitaxial layers and, on a first surface of the epitaxial layers remote from the substrate, a first ohmic contact layer; the first ohmic contact layers being on p-type layers of the epitaxial layers.

25. A method as claimed in any claim 22, wherein the second ohmic contact layer is formed on n-type layers of the expitaxial layers.

26. A method as claimed in any one of claims 1 to 14, wherein after step (c), dielectric films are deposited on the epitaxial layers and openings are cut in the dielectric films and second ohmic contact layer and bond pads deposited on the epitaxial layers.

27. A method as claimed in any one of claims 1 to 14, wherein after step (c), electroplating of a thermally conductive metal on the epitaxial layers is performed.

28. A method as claimed in any one of claims 24 to 27, wherein the thermally conductive metal comprises copper and the epitaxial layers comprise multiple GaN-related layers.

29. A semiconductor device comprising epitaxial layers, first ohmic contact layers on a first surface of the epitaxial layers, a relatively thick layer of a thermally conductive metal on the first ohmic contact layer, and a second

ohmic contact layer on a second surface of the epitaxial layers; the relatively thick layer being applied by electroplating.

30. A semiconductor device as claimed in claim 29, wherein there is an adhesive layer on the first ohmic contact layer between the first ohmic contact layer and the relatively thick layer.

31. A semiconductor device as claimed in claim 30, wherein there is a seed layer of the thermally conductive metal, applied to the adhesive layer.

32. A semiconductor device as claimed in any one of claims 29 to 31, wherein the relatively thick layer is at least 50 micrometers thick.

33. A semiconductor device as claimed in any one of claims 29 to 32, wherein the second ohmic contact layer is a thin layer in the range of from 3 to 500 nanometers.

34. A semiconductor device as claimed in any one of claims 29 to 33, wherein the second ohmic contact layer is selected from the group consisting of: opaque, transparent, and semi-transparent.

35. A semiconductor device as claimed in any one of claims 29 to 34, wherein the second ohmic layer includes bonding pads.

36. A semiconductor device as claimed in any one of claims 29 to 35, wherein the thermally conductive metal is copper and the epitaxial layers comprise multiple GaN-related epitaxial layers.

37. A semiconductor device as claimed in any one of claims 29 to 36, wherein the semiconductor device is selected from the group consisting of: a light emitting device, and a transistor device.

38. A semiconductor device comprising epitaxial layers, a first ohmic contact layer on a first surface of the epitaxial layers, an adhesive layer on the first ohmic contact layer, and a seed layer of a thermally conductive metal on the adhesive layer.

39. A semiconductor device as claimed in claim 38, further including a relatively thick layer of the thermally conductive metal on the seed layer, the relatively thick layer acting as a heat sink.

40. A semiconductor device as claimed in claim 38 or claim 39, further including a second ohmic contact layer on a second surface of the epitaxial layers; the second ohmic contact layer being a thin layer in the range of from 3 to 500 nanometers.

41. A semiconductor device as claimed in any one of claims 38 to 40, wherein the second ohmic contact layer comprises bonding pads and is selected from the group consisting of : opaque, transparent, and semi-transparent.

42. A semiconductor device as claimed in any one of claims 38 to 41, wherein the thermally conductive metal comprises copper; and the epitaxial layers comprise GaN-related layers.

43. A method of fabrication of a semiconductor device, the method including the steps:

(a) on a substrate with a wafer comprising multiple GaN-related epitaxial layers, forming a first ohmic contact layer on a first surface of the wafer;

(b) removing the substrate from the wafer; and

(c) forming a second ohmic contact layer on a second surface of the wafer, the second ohmic contact layer having bonding pads formed thereon.

44. A method as claimed in claim 43, wherein the second ohmic contact layer is selected from the group consisting of: opaque, transparent, and semi-transparent.

45. A method as claimed in claim 43 or claim 44, wherein the second ohmic contact layer is one of: blank, and patterned.

46. A semiconductor device fabricated by the method of any one of claims 43 to 45.

47. A semiconductor device as claimed in claim 46, wherein the semiconductor device is one of: a light emitting device, and a transistor device.

48. A method for fabrication of a semiconductor device on a substrate, the semiconductor device having wafer with a device layer; the method including the steps:

(a) electroplating a layer of a thermally conductive material onto a surface of the wafer remote from the substrate and close to the device layer; and

(b) removing the substrate.

49. A method as claimed in claim 48, wherein the semiconductor device is a silicon-based device.

50. A method for fabrication of a light emitting device on a substrate, the light emitting device having wafer with an active layer; the method including the steps:

(a) electroplating a layer of a thermally conductive material onto a surface of the wafer remote from the substrate and close to the active layer; and

(b) removing the substrate.

51. A method as claimed in any one of claims 48 to 50, wherein the thermally conductive layer is as a heat sink.

52. A method as claimed in claim 51, wherein the thermally conductive layer is of a thickness in the range of from 3 microns to 300 microns.

53. A method as claimed in claim 51 or claim 52, wherein the thermally conductive layer is of a thickness of from 50 to 200 microns.

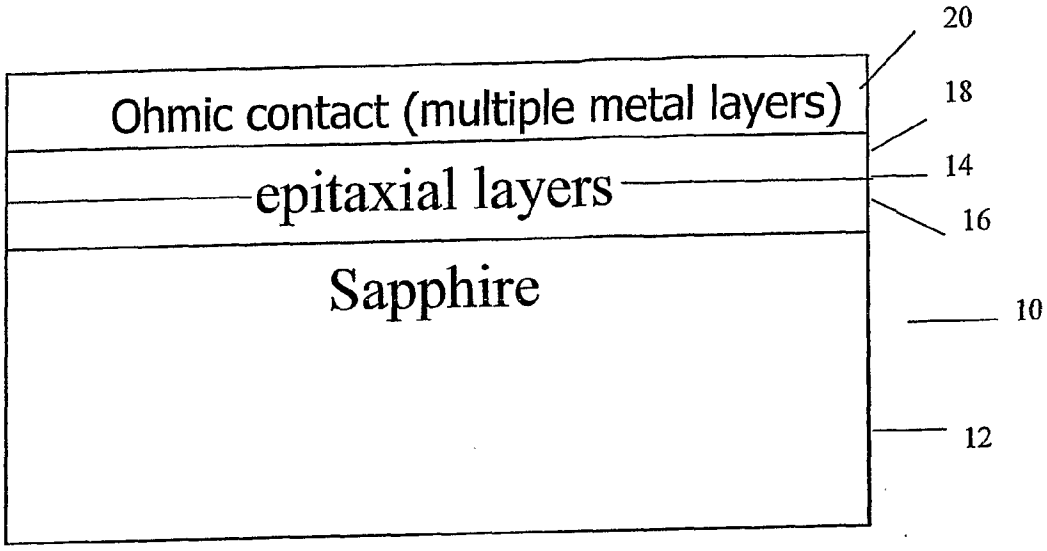

Figure 1

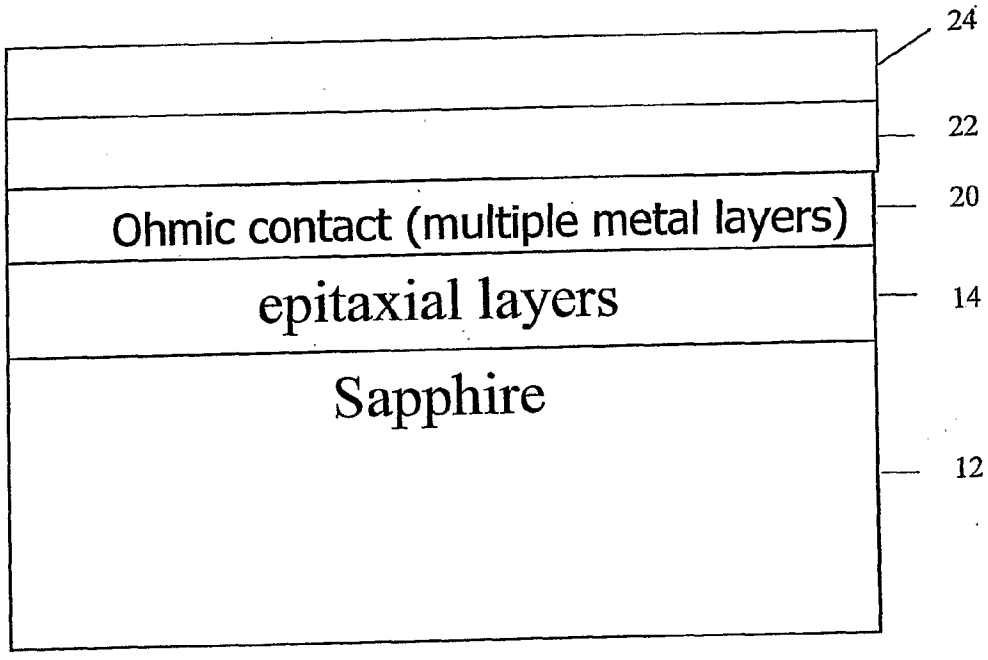

Figure 2

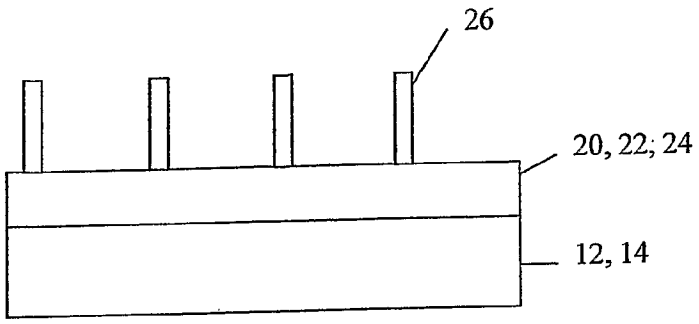

Figure 3

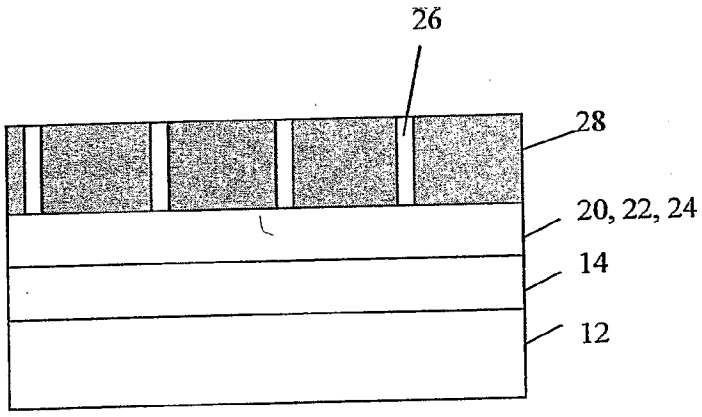

Figure 4

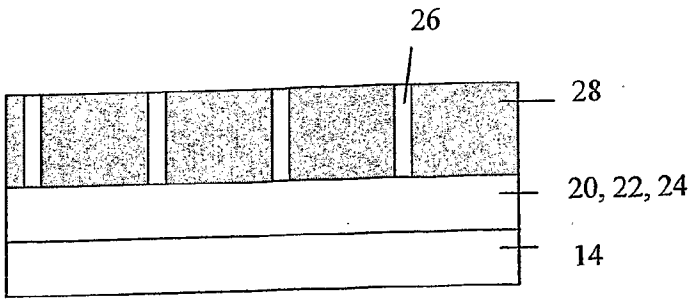

Figure 5

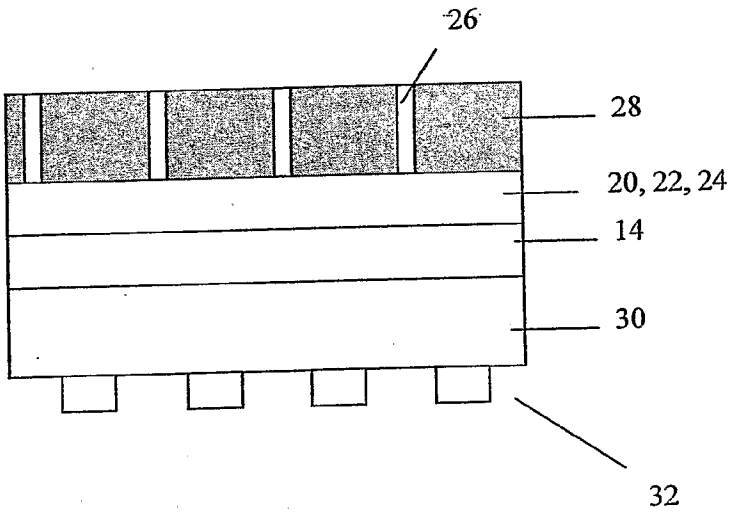

Figure 6

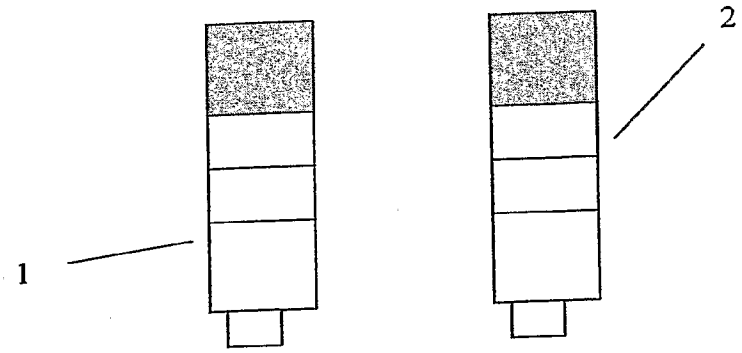

Figure 7

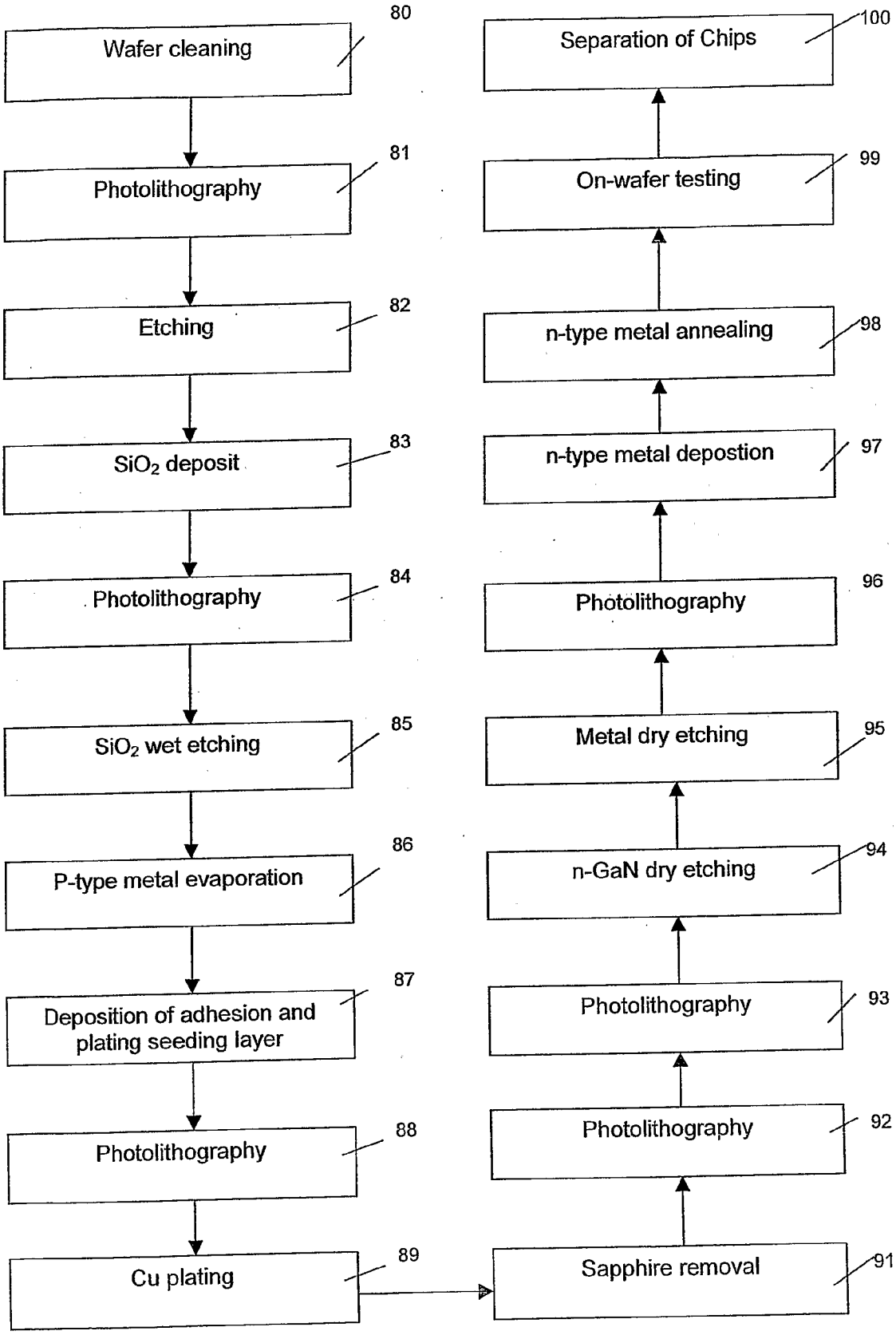
Wafer cleaning
80
Photolithography
81
Etching
82
SiO_2 deposit
83
Photolithography
84
SiO_2 wet etching
85
P-type metal evaporation
86
Deposition of adhesion and plating seeding layer
87
Photolithography
88
Cu plating
89
Sapphire removal
91
Photolithography
92
Photolithography
93
n-GaN dry etching
94
Metal dry etching
95
Photolithography
96
n-type metal depostion
97
n-type metal annealing
98
On-wafer testing
99
Separation of Chips
100

Figure 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG03/00223

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl. [7]: H01L 21/4763, 21/285, 23/36, 23/367, 23/373, 31/024, 31/052, 31/18, H01S 5/024

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
file dwpi: limit /ic h01l-021 or h01l-023 or h01l-031 or h01l-033 or h0 1s-005, gan or (gallium (w) nitride), sapphire or gaas or inp or si, epitax+ or epilayer?, copper or cu, adhesion (w) layer, seed (w) layer, (heat or thermal+) (s) (sink+ or spread+ or conduct+ or dissipat+ or remov+), laser or led? or (light (w) emitting), ohmic (w) contact, active (w) region, thick, electroplat+ or electrodeposit+, lift (w) off, (host or temporary or remov+) (2d) substrate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6562648 B1 (WONG et al.) 13 May 2003 Column 4, lines 3–17; figures 1*a*–1*g*	
A	US 2003/0064535 A1 (KUB et al.) 3 April 2003 Page 2, paragraphs [0032]–[0035]; figures 1*(a)*–1*(d)*	
A	US 6448102 B1 (KNEISSL et al.) 10 September 2002 Column 2, lines 5–38; figures 11*a*–11*f*	

[X] Further documents are listed in the continuation of Box C [X] See patent family annex

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
2 December 2003	09 DEC 2003
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustralia.gov.au Facsimile No. (02) 6285 3929	Authorized officer **RAJEEV DESHMUKH** Telephone No : (02) 6283 2145

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG03/00223

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6210479 B1 (BOJARCZUK et al.) 3 April 2001 Column 3, line 18–column 4, linc52; figures 1–6	
A	EP 1326290 A2 (XEROX CORPORATION) 9 July 2003 Abstract; figure 2	
E, A	US 6627921 B2 (WONG et al.) 30 September 2003 Column 4, lines 10–23; figures 1*a*–1*g*	

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/SG03/00223

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member					
US	6562648	JP	2002076523	US	2003122141		
US	2003064535						
US	6448102	JP	2000196197	US	6365429		
US	6210479	JP	10270712	JP	2000252224	JP	2002198539
		US	5946551	US	5981970	US	6344660
		US	6344662				
EP	1326290	CA	2414325	JP	2003234542	US	6455340
US	6627921	JP	2002076523	US	6562648	US	2003122141

END OF ANNEX